Docket No.: END919980055US4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: G. J. Armezzani et al.

Group Art Unit:	:	IBM Corporation
Examiner:	:	Intellectual Property Law
Serial No.:	:	Dept. N50, Bldg. 040-4
Filed: herewith	:	1701 North Street
Title: ELECTRONIC PACKAGE WITH STACKED CONNECTIONS AND METHOD FOR MAKING SAME	:	Endicott, NY 13760

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner For Patents, Washington, D.C. 20231, on

_____
(Date of Deposit)

_____
Date

Assistant Commissioner For Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above identified application as follows:

IN THE SPECIFICATION:

Page 1, line 8 - before "Background of the Invention", please add:

--Cross Reference to Copending Application

This application is a divisional application of S/N 09/282,842, filed 03/31/99.--

IN THE CLAIMS:

Please cancel all claims and add the following new claims:

1 --26. An electronic package comprising:

a first flexible circuitized substrate having at least one conductive aperture therein having an external surface;

a second flexible circuitized substrate having at least one conductive aperture therein having an external surface, said first and second flexible circuitized substrates aligned such that said at least one conductive aperture of said first flexible circuitized substrate is substantially aligned with said at least one conductive aperture of said second flexible circuitized substrate wherein said first and second flexible circuitized substrates are comprised of a material selected from the group consisting of polyimide, polytetrafluoroethylene, and epoxy glass cloth, said at least one conductive aperture of said first flexible circuitized substrate and said at least one conductive aperture of said second flexible circuitized substrate including a conductive metallic layer thereon selected from the group consisting of copper, nickel, gold, chromium, solder and alloys thereof ; and

at least one solder member including a first contact portion extending from said external surface of said conductive aperture of said first flexible circuitized substrate and a second contact portion extending substantially within both of said aligned conductive apertures of said first and second flexible circuitized substrates to secure said flexible circuitized substrates together, said metallic material of said at least one conductive aperture of said first flexible circuitized substrate and said at least one conductive aperture of said second flexible circuitized substrate including a protective layer thereon, said protective layer selected from the group consisting of benzatriazole, chlorite, and immersion tin.

27. The electronic package of claim 26 wherein said at least one conductive aperture of said first flexible circuitized substrate and said at least one conductive aperture of said second flexible circuitized substrate comprises a hole having a cylindrical shape.

28. The electronic package of claim 26 where said solder member is comprised of a high melt solder alloy having a melting point temperature greater than about 183 degrees Celsius.

29. The electronic package of claim 28 wherein said high melt solder alloy is comprised of metallic material, said metallic material is selected from the group consisting of tin, lead, gold, silver, antimony, and combinations thereof.

30. The electronic package of claim 26 wherein said first contact portion of said solder member extending from said external surface of said conductive aperture of said first flexible circuitized substrate includes a cross-sectional configuration that is substantially round, oval, or ellipsoidal.

31. The electronic package of claim 30 wherein said first contact portion of said solder member extending from said external surface of said conductive aperture of said first flexible circuitized substrate forms a connection to a printed circuit board.

32. The electronic package of claim 26 wherein said second contact portion of said solder member extends at least to said external surface of said conductive aperture of said flexible second flexible circuitized substrate.

33. The electronic package of claim 32 wherein said second contact portion of said solder member is substantially in the form of a dome on said external surface of said conductive aperture of said second flexible circuitized substrate.

34. The electronic package of claim 32 wherein said second contact portion of said solder member is at least one of an array of solder members on said external surface of said conductive aperture of said second flexible circuitized substrate.

35. The electronic package of claim 34 further including at least one integrated circuit chip, said chip being attached to said array of said solder members.

36. The invention of claim 26 wherein said electronic package is a single chip carrier.

37. The invention of claim 26 wherein said electronic package is a multi-chip module including at least two chips.

38. An electronic package comprising:

a first circuitized substrate having at least one conductive aperture therein having an external surface;

a second circuitized substrate having at least one conductive aperture therein having an external surface, said first and second circuitized substrates aligned such that said at least one conductive aperture of said first circuitized substrate is substantially aligned with said at least one conductive aperture of said second circuitized substrate, said at least one conductive aperture of said first circuitized substrate and said at least one conductive aperture of said second circuitized substrate including a conductive metallic layer thereon selected from the group consisting of copper, nickel, gold, chromium, solder and alloys thereof ; and

at least one solder member including a first contact portion extending from said external surface of said conductive aperture of said first circuitized substrate and a second contact portion extending substantially within both of said aligned conductive apertures of said first and second circuitized substrates to secure said circuitized substrates together, wherein said second contact portion of said solder member extends at least to said external surface of said conductive aperture of said second circuitized substrate, said metallic material of said at least one conductive aperture of said first circuitized substrate and said at least one conductive aperture of said second circuitized substrate including a protective layer thereon, said protective layer selected from the group consisting of benzatriazole, chlorite, and immersion tin.

39. The electronic package of claim 38 wherein said second contact portion of said solder member is substantially in the form of a dome on said external surface of said conductive aperture of said second circuitized substrate.

40. The electronic package of claim 38 wherein said second contact portion of said solder member is at least one of an array of solder members on said external surface of said conductive aperture of said second circuitized substrate.

41. The electronic package of claim 40 further including at least one integrated circuit chip, said chip being attached to said array of said solder members.

42. The invention of claim 38 wherein said electronic package is a single chip carrier.

43. The invention of claim 38 wherein said electronic package is a multi-chip module including at least two chips.

44. A single chip carrier comprising:

a first circuitized substrate having at least one conductive aperture therein having an external surface;

a second circuitized substrate having at least one conductive aperture therein having an external surface, said first and second circuitized substrates aligned such that said at least one conductive aperture of said first circuitized substrate is substantially aligned with said at least one conductive aperture of said second circuitized substrate, said at least one conductive aperture of said first circuitized substrate and said at least one conductive aperture of said second circuitized substrate including a conductive metallic layer thereon selected from the group consisting of copper, nickel, gold, chromium, solder and alloys thereof ;

at least one solder member including a first contact portion extending from said external surface of said conductive aperture of said first circuitized substrate and a second contact portion extending substantially within both of said aligned conductive apertures of said first and second circuitized substrates to secure said circuitized substrates together wherein said second contact portion of said solder member is at least one of an array of solder members on said external surface of said conductive aperture of said second circuitized substrate, said metallic material of said at least one conductive aperture of said first circuitized substrate and said at least one conductive aperture of said second circuitized substrate including a protective layer thereon, said protective layer selected from the group consisting of benzatriazole, chlorite, and immersion tin; and

at least one chip attached to said array of solder members.

45. A multichip module comprising:

a first circuitized substrate having at least one conductive aperture therein having an external surface;

a second circuitized substrate having at least one conductive aperture therein having an external surface, said first and second circuitized substrates aligned such that said at least one conductive aperture of said first circuitized substrate is substantially aligned with said at least one conductive aperture of said second circuitized substrate, said at least one conductive aperture of said first circuitized substrate and said at least one conductive aperture of said second circuitized substrate including a conductive metallic layer thereon selected from the group consisting of copper, nickel, gold, chromium, solder and alloys thereof ;

at least one solder member including a first contact portion extending from said external surface of said conductive aperture of said first circuitized substrate and a second contact portion extending substantially within both of said aligned conductive apertures of said first and second circuitized substrates to secure said circuitized substrates together wherein said second contact portion of said solder member is at least one of an array of solder members on said external surface of said conductive aperture of said second circuitized substrate said metallic material of said at least one conductive aperture of said first circuitized substrate and said at least one conductive aperture of said second circuitized substrate including a protective layer thereon, said protective layer selected from the group consisting of benzatriazole, chlorite, and immersion tin; and

at least two chips attached to said array of solder members.--

REMARKS

The specification is amended to reference the parent application, SN 09/282,842.

Claims 1-25 are cancelled. Claims 26-45 have been added. New independent claim 26 recites the subject matter of original independent structure claim 1 and includes all the limitations of original claims 2, 3, and 5-8. Note claims 26-45 are similar to claims 42-63 submitted 9/18/00 by Applicants in SN 09/282,842, but subsequently cancelled following a phone discussion with the Examiner. New dependent claims 27 and 30-34 recite the subject matter of original claims 4 and 11-15 and include the limitation that the first and second circuitized substrates are "flexible" consistent with allowable independent claim 26 from which these depend. New dependent claims 28, 29, and 35-37, recite the subject matter of original claims 9, 10, and 16-18 and depend from allowable subject matter. New independent claim 38 recites the subject matter of original claims 1, 5-8 and 13. New dependent claims 39-43 recite the subject matter of original claims 14-18 and depend from new allowable independent claim 38. New independent claim 44 recites the subject matter of original claims 1, 5-8, and 15-17 including the added feature of a chip coupled to the defined array. New independent claim 45 recites the subject matter of original claims 1, 5-8, 15-16, and 18, further including the added feature of at least two chips coupled to the defined array.

Support being fully provided for all the above amending, this amending does not constitute the addition of new matter and entry is urged.

Copies of the IDS and PTO-1449 form mailed on 3/31/99 in the parent application, S/N 09/282,842, are included herewith. Upon request, copies of these documents will be provided.

The Application is deemed in condition for allowance and such action on the part of the Examiner is respectfully requested. Should the Examiner believe, however, that minor

differences remain which, if overcome, would result in allowance of the Application and that said differences can be openly discussed in a phone conversation, the Examiner is cordially requested to phone the undersigned, collect, at the number provided below, for the purpose of discussing these differences and hopefully obtaining allowance of the Application.

Respectfully submitted,

Dated: Jan. 15, 2001

By: _____
Lawrence R. Fraley
Reg. No. 26,885

Telephone: (607)755-3207
Fax: (607)755-3250